AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A scan test control method for a scan test circuit, said scan test circuit having

a scan chain including n pieces of scan storage elements in which n is an integer that is greater than 1 ~~(n: integer, n>1)~~ and

a storage element which is provided in front of the scan chain, wherein the method includes the steps of:

independently controlling a frequency of a first clock to be used for shifting data into the storage element and the first to ~~(n-1)~~ n -1 th scan storage elements, and

independently controlling a frequency of a second clock to be used for shifting data into the n[-]th scan storage element and performing normal operation~~, are independently controlled~~.

2. (Original) The scan test control method of Claim 1, wherein the frequency of the first clock and the frequency of the second clock are different from each other.

3. (Original) The scan test control method of Claim 1, wherein the frequency of the second clock is a clock frequency to be used in the normal operation.

4. (Currently Amended) A scan test circuit comprising:

a scan chain having n pieces of scan storage elements ~~(n: integer, n>1)~~ in which n is an integer that is greater than 1;

a storage element that is provided in front of the scan chain;

a scan clock generation circuit for receiving first and second clocks, and outputting one of the first clock and the second clock as a scan clock for operating the plural scan storage elements and the storage element; and

a selection circuit for selecting the first clock as the scan clock to be used for shifting data into the storage element and the first to ~~(n-1)~~ n – 1th scan storage elements, and selecting the second clock as the scan clock to be used for shifting data into the n[[-]]th scan storage element and performing normal operation.

5. (Original) The scan test circuit of Claim 4 further including a scan selection signal generation circuit which receives, from the outside, a scan selection external signal for switching between normal operation and scan test operation, and generates a scan selection internal signal for selectively switching between normal operation and operation for shifting data into the plural scan storage elements in synchronization with the second clock.

6. (Original) The scan test circuit of Claim 5, wherein the scan selection signal generation circuit generates a control signal for generating an arbitrary number of the second clocks.

7. (Original) The scan test circuit of Claim 6, wherein the scan selection signal generation circuit switches between a first timing at which the scan clock generation circuit generates the second clock as the scan clock, and a second timing at which the scan selection internal signal is generated.

8. (Original) The scan test circuit of Claim 7, wherein the scan selection signal generation circuit arbitrarily selects one of the first timing and the second timing.

9. (Canceled).

10. (Currently Amended) ~~The scan test circuit of Claim 9, wherein~~
A scan test control method for a scan test circuit, said scan test circuit comprising:
a scan chain having n pieces of scan storage elements, in which n is an integer that is greater than 1;
a storage element that is provided in front of the scan chain;
a scan clock generation circuit for receiving first and second clocks, said method including the step of
outputting one of the first clock and the second clock as a scan clock for operating the plural scan storage elements and the storage element;

a selection circuit for selecting the first clock as the scan clock to be used for shifting data into the storage element and the first to n-1th scan storage elements, and in which the method further includes the step of

selecting the second clock as the scan clock to be used for shifting data into the n[[-]]th scan storage element and performing normal operation; and

a scan selection signal generation circuit which receives, from the outside, a scan selection external signal for switching between normal operation and scan test operation, wherein according to the method a scan selection internal signal is generated by said scan selection signal generation circuit for selectively switching between normal operation and operation for shifting data into the plural scan storage elements in synchronization with the second clock; and in which the method further includes the steps of

replacing when generating a scan test pattern, the scan clock generation circuit ~~is replaced~~ with a circuit that connects a terminal to which the first clock is input, directly to a signal line from which the scan clock is output,

replacing the scan selection signal generation circuit ~~is replaced~~ with a circuit that connects a terminal to which the scan selection external signal is input, directly to a signal line from which the scan selection internal signal is output, and

replacing the storage element ~~is replaced~~ with a circuit that connects a signal line to which data in the storage element is input, directly to a signal line from which the data is output.

11. (Currently Amended) A scan test control method for a scan test circuit, said scan test circuit comprising

a first block having a first scan test circuit that operates in synchronization with first and second clocks, and

a second block having a second scan test circuit that is synchronized with only the first clock,

wherein according to the method,

the first block receives a first scan selection signal that is synchronized with the second clock and indicates switching timing between normal operation and scan test operation of the first scan test circuit, and
the second block receives a second scan selection signal that is synchronized with the first clock and indicates switching timing between normal operation and scan test operation of the second scan test circuit,

wherein the normal operation time of the scan test in the first block is different from the normal operation time of the scan test in the second block.

12. (Original) A scan test circuit comprising a first block having a first scan test circuit that operates in synchronization with first and second clocks, and a second block having a second scan test circuit that is synchronized with only the first clock, said scan test circuit comprising:

a plurality of first storage elements synchronized with the first clock,

a plurality of second storage elements synchronized with the first and second clocks,

a selection circuit for selecting either a first path between the plural first storage elements and the second block, or a second path between the plural second storage elements and the first block, as a path for passing data from the first block to the second block, and

said first storage elements, second storage elements, and selection circuit being provided between the first block and the second block.

13. (Original) The scan test circuit of Claim 12, wherein the plurality of first storage elements and the plurality of second storage elements are a plurality of controllable scan storage elements for controlling a signal inputted to the second block, or a plurality of monitor storage elements for holding a signal outputted from the first block.

14. (Original) The scan test circuit of Claim 13, wherein the plurality of monitor storage elements are constituted by a single monitor storage element.

15. (Original) The scan test circuit of Claim 14, wherein the selection circuit is replaced with a circuit which separates the first path from the second path, when generating a scan test pattern.